We claim:

1. A semiconductor device comprising a semiconductor body having a first device region of one conductivity type forming with a second device region of the opposite conductivity type provided adjacent one of the major surfaces of the semiconductor body a first pn junction which is reverse-biassed in at least one mode of operation of the device, and a floating further region of the opposite conductivity type provided within the first device region remote from the major surfaces of the semiconductor body and spaced from and extending substantially entirely beneath the second device region so that, in the one mode of operation of the device, the depletion region of the first pn junction reaches the floating further region before the first pn junction breaks down, characterized in that the further region forms a further pn junction with a highly-doped capping region of the one conductivity type provided within the first device region between the floating further region and the second device region and spaced from the second device region, and in that an array of floating further regions each forming a further pn junction with a respective highly doped capping region of the one conductivity type is provided within the first device region, with the floating further regions being equally spaced from the first pn junction and being everywhere spaced from one another by a distance sufficient to avoid merging of the depletion regions associated with the further regions under zero bias, the capping regions being everywhere spaced from one another.

2. A semiconductor device according to claim 1, further characterized in that the first device region extends towards the other major surface of the semiconductor body.

3. A semiconductor device according to claim 1, further characterized in that a third device region of the one conductivity type is provided within the second device region.

4. A semiconductor device according to claim 3, further characterized in that the first device region forms at least part of the collector region of a bipolar transistor with the second and third device regions forming the base and emitter regions, respectively.

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